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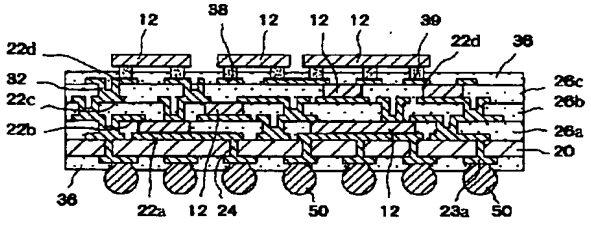
(54)【発明の名称】　半導体装置及びその製造方法

(57)【要約】
【課題】　半導体素子を集積して半導体装置に搭載することを可能にし、コンパクトで複合機能を有する半導体装置を提供する。
【解決手段】　基板３０上に絶縁層２６ａ、２６ｂ、２６ｃを介して配線パターン２２ａ、２２ｂ、２２ｃ、２２ｄが多層に積層され、該配線パターンが層間で電気的に接続されてなる半導体装置において、前記配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子１２が埋設されて搭載されている。内層の配線層は、下層の配線パターンを被覆するとともに、電極端子形成面を上面にして内層に搭載された半導体素子１２の側面を封止する、半導体素子の厚さと略同じ厚さの絶縁層２６ａ、２６ｂ、２６ｃ、２６ｄと、絶縁層を貫通して形成されたビア３２を介して下層の配線パターンと電気的に接続されるとともに、該絶縁層の表面に形成され、前記半導体素子の電極端子形成面上に延出して該電極端子と電気的に接続される上層の配線パターンとを備えている。



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【特許請求の範囲】

【請求項１】　基板上に絶縁層を介して配線パターンが多層に積層され、該配線パターンが層間で電気的に接続されてなる半導体装置において、

前記配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子が埋設されて搭載されていることを特徴とする半導体装置。

【請求項２】　内層の配線層が、下層の配線パターンを被覆するとともに、電極端子形成面を上面にして内層に搭載された半導体素子の側面を封止する、半導体素子の厚さと略同じ厚さの絶縁層と、

該絶縁層を貫通して形成されたビアを介して下層の配線パターンと電気的に接続されるとともに、該絶縁層の表面に形成され、前記半導体素子の電極端子形成面上に延出して該電極端子と電気的に接続される上層の配線パターンとを備えていることを特徴とする請求項１記載の半導体装置。

【請求項３】　基板の両面に前記配線パターンが形成され、基板を貫通して設けた導通部を介して基板の両面に設けられた配線パターンが電気的に接続されていることを特徴とする請求項１または２記載の半導体装置。

【請求項４】　基板が金属板によって形成され、該金属板の一方の面側の内層に半導体素子を埋設した配線層が形成されていることを特徴とする請求項１または２記載の半導体装置。

【請求項５】　配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子が埋設されて搭載された半導体装置の製造方法において、

下層の配線パターンを有する配線層に電極端子形成面を上面にして半導体素子を搭載し、

下層の配線パターンと半導体素子の側面とを絶縁層により被覆し、

該絶縁層を貫通して前記下層の配線パターンを露出させるビア穴を形成し、ビア穴の内面、絶縁層の表面及び半導体素子の表面に電解めっき用のめっき給電層を形成した後、

該めっき給電層上に配線パターンを形成する部位を露出したレジストパターンを形成し、該レジストパターンをマスクとして電解めっきを施し、

次いで、前記レジストパターンを除去した後、該レジストパターンの除去によって露出しためっき給電層部分を除去して、下層の配線パターンと上層の配線パターンとを電気的に接続するビアと、前記半導体素子の電極端子と電気的に接続する上層の配線パターンとを形成することを特徴とする半導体装置の製造方法。

【請求項６】　配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子が埋設されて搭載された半導体装置の製造方法において、

基板、あるいは下層の配線パターンを被覆して形成した絶縁層に電極端子形成面を上面にして半導体素子を搭載し、

半導体素子の側面を絶縁層により被覆し、

該絶縁層を貫通して前記下層の配線パターンを露出させるビア穴を形成し、ビア穴の内面、絶縁層の表面及び半導体素子の表面に電解めっき用のめっき給電層を形成した後、

該めっき給電層上に配線パターンを形成する部位を露出したレジストパターンを形成し、該レジストパターンをマスクとして電解めっきを施し、

次いで、前記レジストパターンを除去した後、該レジストパターンの除去によって露出しためっき給電層部分を除去して、下層の配線パターンと上層の配線パターンとを電気的に接続するビアと、前記半導体素子の電極端子と電気的に接続する上層の配線パターンとを形成することを特徴とする半導体装置の製造方法。

【請求項７】　半導体素子を所定位置に搭載した後、半導体素子の厚さと略同じ厚さに形成され、半導体素子を収納する素子収納孔が形成された絶縁樹脂フィルムを、半導体素子と素子収納孔とを位置合わせして配置し、

リリースフィルムを介して前記絶縁樹脂フィルムを加熱・加圧して半導体素子を搭載した層に絶縁層を形成することを特徴とする請求項５記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は単一のパッケージ内に複数の半導体素子を搭載した半導体装置及びその製造方法に関するものである。

【０００２】

【従来の技術】半導体装置の高集積化、高機能化を図る目的で単一のパッケージ内に複数の半導体素子を搭載した半導体装置が従来提供されている。図７は一枚の基板１０に半導体素子１２を複数個搭載した半導体装置の例を示す。図７(a) は基板１０の両面に半導体素子１２を搭載した例、図７(b) は基板１０の片面に半導体素子１２を積み重ねて搭載した例、図７(c) は基板１０の平面内に半導体素子１２を複数個搭載した例、図７(d) は基板１０の両面に半導体素子１２を搭載すると共に基板の平面内に半導体素子１２を複数個搭載した例である。

【０００３】基板１０の表面には配線パターンが形成されており、図示例ではいずれも半導体素子１２と配線パターンとをワイヤボンディングによって電気的に接続している。もちろん、半導体素子１２と配線パターンとの電気的接続はワイヤボンディング接続に限らず、フリップチップ接続、ＴＡＢ接続等が利用できる。

【０００４】

【発明が解決しようとする課題】上記の半導体装置は基板１０の搭載面内に半導体素子１２を搭載するから、半導体素子１２の搭載数が制限されるし、半導体素子１２を積み重ねて搭載する場合でも何枚も積層することがで

きない。また、半導体素子１２と基板１０の配線パターンとをワイヤボンディングによって接続する場合は、ボンディングエリアが必要となるから、さらに半導体素子１２を搭載する面積が狭くなる。

【０００５】このようにパッケージ内に複数の半導体素子１２を搭載する場合に、単に基板１０の搭載面に半導体素子１２を搭載する方法では半導体素子１２の搭載数が限定され十分な高集積化及び高機能化を図ることができない。そこで、さらに半導体装置の高集積化及び高機能化を図る方法として、基板を多層化し基板内に半導体素子を内蔵する形式の半導体装置が考えられている。図８は樹脂基体１４中に半導体素子１２を埋設し、半導体素子１２の電極端子形成面上に配線層１６を形成して成る半導体装置である。

【０００６】このように、複数の配線層を備えた多層基板の構造を利用すれば、半導体素子等のチップ状の部品を相互に電気的に接続して、基板内で３次元的に配置することが可能である。しかしながら、基板内に半導体素子を埋設し、かつ配線層を多層に形成することは必ずしも容易ではなく、また、全体の厚さを薄くして、半導体装置をコンパクトに形成しなければならないという問題もある。本発明はこのような単一のパッケージ内に複数の半導体素子を搭載した半導体装置に係るものであり、その目的とするところは、従来の半導体装置にくらべて効果的に高集積化及び高機能化を図ることができ、確実に、かつコンパクトに製造することができる半導体装置及びその製造方法を提供するにある。

【０００７】

【課題を解決するための手段】上記目的を達成するため、本発明は次の構成を備える。すなわち、基板上に絶縁層を介して配線パターンが多層に積層され、該配線パターンが層間で電気的に接続されてなる半導体装置において、前記配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子が埋設されて搭載されていることを特徴とする。また、内層の配線層が、下層の配線パターンを被覆するとともに、電極端子形成面を上面にして内層に搭載された半導体素子の側面を封止する、半導体素子の厚さと略同じ厚さの絶縁層と、該絶縁層を貫通して形成されたビアを介して下層の配線パターンと電気的に接続されるとともに、該絶縁層の表面に形成され、前記半導体素子の電極端子形成面上に延出して該電極端子と電気的に接続される上層の配線パターンとを備えていることを特徴とする。また、基板の両面に前記配線パターンが形成され、基板を貫通して設けた導通部を介して基板の両面に設けられた配線パターンが電気的に接続されていることを特徴とする。また、基板が金属板によって形成され、該金属板の一方の面側の内層に半導体素子を埋設した配線層が形成されていることを特徴とする。

【０００８】また、配線パターンが形成された内層の配線層に、該配線パターンと電気的に接続された半導体素子が埋設されて搭載された半導体装置の製造方法において、下層の配線パターンを有する配線層に電極端子形成面を上面にして半導体素子を搭載し、下層の配線パターンと半導体素子の側面とを絶縁層により被覆し、該絶縁層を貫通して前記下層の配線パターンを露出させるビア穴を形成し、ビア穴の内面、絶縁層の表面及び半導体素子の表面に電解めっき用のめっき給電層を形成した後、該めっき給電層上に配線パターンを形成する部位を露出したレジストパターンを形成し、該レジストパターンをマスクとして電解めっきを施し、次いで、前記レジストパターンを除去した後、該レジストパターンの除去によって露出しためっき給電層部分を除去して、下層の配線パターンと上層の配線パターンとを電気的に接続するビアと、前記半導体素子の電極端子と電気的に接続する上層の配線パターンとを形成することを特徴とする。また、前記半導体装置の製造方法において、基板、あるいは下層の配線パターンを被覆して形成した絶縁層に電極端子形成面を上面にして半導体素子を搭載し、半導体素子の側面を絶縁層により被覆し、該絶縁層を貫通して前記下層の配線パターンを露出させるビア穴を形成し、ビア穴の内面、絶縁層の表面及び半導体素子の表面に電解めっき用のめっき給電層を形成した後、該めっき給電層上に配線パターンを形成する部位を露出したレジストパターンを形成し、該レジストパターンをマスクとして電解めっきを施し、次いで、前記レジストパターンを除去した後、該レジストパターンの除去によって露出しためっき給電層部分を除去して、下層の配線パターンと上層の配線パターンとを電気的に接続するビアと、前記半導体素子の電極端子と電気的に接続する上層の配線パターンとを形成することを特徴とする。また、半導体素子を所定位置に搭載した後、半導体素子の厚さと略同じ厚さに形成され、半導体素子を収納する素子収納孔が形成された絶縁樹脂フィルムを、半導体素子と素子収納孔とを位置合わせして配置し、リリースフィルムを介して前記絶縁樹脂フィルムを加熱・加圧して半導体素子を搭載した層に絶縁層を形成することを特徴とする。

【０００９】

【発明の実施の形態】以下、本発明の好適な実施形態を添付図面に基づいて詳細に説明する。図１、２は本発明に係る半導体装置の製造方法を工程順に示す説明図である。本実施形態では樹脂基板の両面に銅箔を貼った両面銅貼り基板を基板に使用して多層に配線層を形成する。基板として樹脂基板以外に金属基板やメタルコア基板等を使用することも可能であるが、以下では、まず、樹脂基板を基板材料とする基板を用いて半導体装置を形成する方法について説明する。

【００１０】図１(a) は樹脂基板２０の一方の面と他方の面に配線パターン２２ａ、２３が形成され、これらの配線パターン２２ａ、２３が樹脂基板２０を厚さ方向に

貫通する導通部２４を介して電気的に接続された基板３０を示す。基板３０は、両面銅貼り基板に貫通孔を形成し、無電解銅めっき及び電解銅めっきを施して貫通孔の内壁面に導体膜を形成し、貫通孔に樹脂を充填した後、樹脂基板２０の表面の銅箔とめっきにより銅箔上に形成されためっき層からなる導体層をエッチングし配線パターン２２ａ、２３を形成して得られる。貫通孔の内壁面に形成される導体膜が配線パターン２２ａ、２３を電気的に接続する導通部２４となる。

【００１１】なお、基板３０は樹脂基板２０の両面に配線パターンを複数層に形成したもの、たとえば4層の配線層を有するもの等であってもよい。基板３０は多層配線基板でのコア基板として作用する。複数層に配線層を形成した基板は、下層の配線パターンを形成した後、絶縁層により配線パターンを被覆し、レーザ光照射等により絶縁層にビア穴を形成し、ビア穴の内面を含む絶縁層の表面を導体層によって被着し、導体層を所要のパターンにエッチングして得られる。なお、別の方法として、樹脂基板に貫通孔をあける工程を配線パターンを絶縁層によって被覆した後の工程とし、絶縁層を含めて貫通孔を形成した後、貫通孔の内壁面に導体部を形成しあわせて絶縁層の表面に導体層を形成し、導体層をエッチングして上層の配線パターンを形成する方法もある。

【００１２】図１(b) は次に、基板３０に半導体素子１２を搭載した状態である。半導体素子１２は機能面を上面側として第１層の配線層に搭載する。配線パターン２２ａは半導体素子１２の搭載位置を考慮し、また上層の配線パターンとの電気的接続を考慮して所定のパターンに形成されている。たとえば、配線パターン２２ａの形成方法として、半導体素子１２の搭載部が接地電位となるように配線パターン２２ａを形成するといったことができる。図のように、半導体素子１２は、基板３０の平面範囲内で複数個所に搭載する。

【００１３】本実施形態の半導体装置は基板３０の一方の面のみに半導体素子１２を積層するように形成するものであり、本実施形態で基板３０の下面に設けた配線パターン２３ははんだボール等の外部接続端子を接合するランドとして形成される。もちろん、製品形態により、基板３０の両面に半導体素子１２を搭載することが可能である。半導体素子１２は基板内に積層して配置するからできるだけ厚さの薄いものを使用する。現在、半導体素子として５０μｍ～１００μｍ程度の厚さのものが提供されている。この程度の厚さの半導体素子１２であれば基板内に積層して埋設して使用することは十分に可能である。

【００１４】図１(c) は、次に、第１層の配線パターン２２ａを絶縁層２６ａによって被覆した状態である。２８は層間で配線層を電気的に接続するビアを形成するためのビア穴である。本実施形態では絶縁層２６ａを形成する際に、半導体素子１２の厚さと略同じ厚さに絶縁層２６ａを形成し、半導体素子１２の電極端子形成面（上面）が絶縁層２６ａによって被覆されないように形成することが特徴である。半導体素子１２と配線パターンとは絶縁層２６ａの表面に形成する導体層を介して電気的に接続するようにするからである。

【００１５】半導体素子１２の電極端子形成面を絶縁層２６ａによって被覆しないようにするため、絶縁層２６ａを形成する絶縁樹脂フィルム４０として半導体素子１２の搭載位置に合わせて素子収納孔４０ａを形成したフィルムを使用する。図３に絶縁樹脂フィルム４０を基板に接着する方法を示す。素子収納孔４０ａを形成した絶縁樹脂フィルム４０を基板に位置合わせし（図３(a)）、基板に配置する（図３(b)）。絶縁樹脂フィルム４０に素子収納孔４０ａが形成されているから半導体素子１２の電極端子形成面を被覆せずに絶縁樹脂フィルム４０が配置される。

【００１６】絶縁樹脂フィルム４０を基板に配置した後、絶縁樹脂フィルム４０を加熱・加圧して絶縁層２６ａを形成する（図３(c)）。この加熱・加圧操作は絶縁樹脂フィルム４０を確実に接着することと、絶縁層２６ａの表面を半導体素子１２の表面と同一の高さの平坦面にすることを目的とする。実施形態では絶縁樹脂フィルム４０と半導体素子１２の表面をリリースフィルム４２によって被覆し、リリースフィルム４２を介して熱板４４により加熱・加圧して半導体素子１２の側面部分を封止する。リリースフィルム４２を介して熱圧着するのは、絶縁樹脂フィルム４０を加熱・加圧して接着する際に半導体素子１２の電極端子形成面が汚染されないようにするためである。

【００１７】リリースフィルム４２は所要の耐熱性を有し、絶縁樹脂フィルム４０（絶縁層２６ａ）、半導体素子１２と容易に剥離できるものを使用する。絶縁樹脂フィルム４０としては、たとえば接着性を有するポリイミド樹脂が使用できる。絶縁樹脂フィルム４０に形成する素子収納孔４０ａは半導体素子１２と同寸か、もしくはやや大きく形成する。また、絶縁樹脂フィルム４０は半導体素子１２の厚さと同じか、もしくはやや厚いものを使用する。絶縁層２６ａを形成した後、絶縁層２６ａの所要部位にレーザ光を照射し、底面に配線パターン２２ａが露出するビア穴２８を形成する。こうして、図１(c)に示すビア穴２８が形成された絶縁層２６ａが得られる。

【００１８】図１(d) は、絶縁層２６ａの表面に第２層の配線パターン２２ｂを形成した状態である。第２層の配線パターン２２ｂは次のような方法によって形成することができる。まず、絶縁層２６ａに無電解銅めっきあるいはスパッタリングを施してビア穴２８を含む絶縁層２６ａの表面及び半導体素子１２の表面に、電解めっきを施すめっき給電層としての薄い導電層を形成する。次に、この薄い導電層の表面に感光性レジストを塗布し、

第２層の配線パターン２２ｂを形成する部位を露出したレジストパターンを形成する。次に、このレジストパターンをめっき用のマスクとし、薄い導電層をめっき給電層として電解銅めっきを施し肉厚の導体層を形成する。導体層を形成した後、先の電解めっきで使用したレジストパターンを除去し、薄いめっき給電層の露出部分をエッチングにより除去し肉厚の導体層を残す。こうして、絶縁層２６ａに配線パターン２２ｂが形成される。

【００１９】ビア穴２８では穴の内面に導体層が被着して形成され、第１層の配線パターン２２ａと第２層の配線パターン２２ｂとを電気的に接続するビア３２が形成される。また、半導体素子１２の電極端子形成面では半導体素子１２の電極端子と電気的に接続する接続パターン３４が形成される。接続パターン３４は半導体素子１２の電極端子形成面上に延出して電極端子に接続するように形成する。前述したように、絶縁層２６ａの表面と半導体素子１２の電極端子形成面とは同一高さの平坦面に形成されているから、めっき給電層用の薄い導電層を形成した後、めっき用のレジストパターンを用いて電解めっきを施すことにより配線パターンと同時に接続パターン３４が形成される。なお、接続パターン３４は当該配線層での配線パターンの一部となるものであり、当該配線層での引き回し用のパターンと半導体素子１２に接続される接続パターン３４をともに含む意味で配線パターンという。

【００２０】図１(e) は、第２層の配線パターン２２ｂに半導体素子１２を搭載した状態である。第１層の配線パターン２２ａに半導体素子１２を搭載した方法と同様に、電極端子形成面を上面にし、配線パターン２２ｂに位置合わせして半導体素子１２を搭載する。図１(f) は、次に、第２層の配線パターン２２ｂを絶縁層２６ｂによって被覆した状態である。絶縁層２６ｂも絶縁層２６ａを形成したと同様に、半導体素子１２の配置に合わせて素子収納孔を設けた絶縁樹脂フィルムを熱圧着し、半導体素子１２の電極端子形成面と絶縁層２６ｂの表面とが同一高さの平坦面となるように形成する。２８は絶縁層２６ｂに形成したビア穴である。

【００２１】図２(a) は、絶縁層２６ｂの表面に第３層目の配線パターン２２ｃを形成した状態である。３２が第２層目の配線パターン２２ｂと第３目の配線パターン２２ｃとを電気的に接続するビアである。配線パターン２２ｃには、第２層目の場合と同様に、半導体素子１２の電極端子と電気的に接続する接続パターン３４を形成する。図２(b) は、第３層目の配線パターン２２ｃに半導体素子１２を搭載した状態である。この場合も、電極端子形成面を上面にして半導体素子１２を搭載する。図２(c) は、配線パターン２２ｃを絶縁層２６ｃによって被覆した状態である。半導体素子１２の電極端子形成面と絶縁層２６ｃの表面とが面一の平坦面になるよう絶縁層２６ｃを形成する。

【００２２】図２(d) は、絶縁層２６ｃの表面に導体層を形成し、導体層をエッチングして第４層の配線パターン２２ｄを形成した状態である。第４層の配線パターン２２ｄもビア３２を介して第３層の配線パターン２２ｃと電気的に接続され、接続パターン３４を介して半導体素子１２と電気的に接続される。図２(e) は、第４層の配線パターン２２ｄを形成した後、第４層の配線パターン２２ｄの表面を保護膜のソルダーレジスト３６によって被覆し、基板３０の下面の配線パターン２３をソルダーレジスト３６によって被覆する。配線パターン２２ｄの表面を被覆するソルダーレジスト３６は、最上層に搭載する半導体素子の接続端子の配置位置に合わせて底面で配線パターン２２ｄが露出する接続部３８を設けたものである。一方、配線パターン２３を被覆するソルダーレジスト３６はランド２３ａが底面で露出するように設けたものである。接続部３８及びランド２３ａの表面には金めっき等の保護めっきが施される。

【００２３】図２(e) に示す多層配線基板は内層に半導体素子１２が配置されるとともに、樹脂基板２０を基板として層間で電気的に接続した複数の配線層が形成されたものとなる。図４は図２(e) に示す多層配線基板で、最上層の配線パターン２２ｄにバンプ３９を介して半導体素子１２を搭載し、配線パターン２３のランド２３ａに外部接続端子５０としてはんだボールを接合して得た半導体装置の最終形状を示す。樹脂基板２０の一方の面上に多層に配線層が形成され、これらの配線層中に半導体素子１２が埋め込まれるとともに、樹脂基板２０の他方の面にこれらの半導体素子１２と電気的に接続する外部接続端子５０が取り付けられている。

【００２４】この半導体装置は外観上は配線基板の一方の面に半導体素子１２が搭載され、他方の面に実装用の外部接続端子が接合されたものとなっているが、多層形成された配線基板の内部に半導体素子１２が内蔵されて構成されていることから、半導体素子１２の集積度がきわめて高度に達成され、複合機能を有するコンパクトな半導体装置として提供することが可能になる。また、製造方法も絶縁層を介して配線層を多層に形成する従来方法を利用するものであり、配線層中に埋設した半導体素子１２と配線パターンとの電気的接続が確保でき、半導体装置としての所要の信頼性を得ることが可能になる。

【００２５】図５は本発明に係る半導体装置の他の実施形態を示す。図５に示す半導体装置は内層に半導体素子１２を埋設して基板３０の一方の面上のみに配線層を形成するとともに、多層に形成した配線層の外面に外部接続端子５０であるはんだボールを接合したことと、隣接する配線層の層間に絶縁層２６を設けたことを特徴とする。隣接する配線層の層間に絶縁層２６を設けたことにより、隣接層での半導体素子１２の配置位置の制約が緩和され、隣接層で半導体素子１２が重複する平面配置とすることが可能になる。

【００２６】図６は図５に示す半導体装置を製造する工程を示す。図６(a)は基板３０に電極端子形成面を上面側として半導体素子１２を搭載し、半導体素子１２の側面間を絶縁層２６によって封止し、絶縁層２６の表面と半導体素子１２の表面に配線パターン２２を形成した状態である。配線パターン２２には半導体素子１２の電極端子に接続する接続パターン３４が形成される。このように半導体素子１２は基板３０に直接搭載することも可能である。絶縁層２６は上述した実施形態と同様に、半導体素子１２の配置位置に合わせて素子収納孔を形成した絶縁樹脂フィルム４０を基板３０上に配置し、リリースフィルムを介して加熱・加圧することにより半導体素子１２の側面を封止するとともに、半導体素子１２の表面と同一高さの平坦面となるように形成する。

【００２７】配線パターン２２は絶縁層２６および半導体素子１２の表面にめっき給電層を設け、めっき給電層の表面に配線パターン２２を形成するためのレジストパターンを設け、このレジストパターンをマスクとして電解めっきを施し、レジストパターンを除去して、薄いめっき給電層の露出部分をエッチングして除去することによって形成できる。図６(b)は配線パターン２２を設けた面を絶縁層２６によって被覆し、下層の配線パターン２２が底面で露出するビア穴２８を形成した状態である。絶縁層２６は絶縁樹脂フィルム４０を被覆し、電気的絶縁性を有する樹脂を薄くコーティングすることによって形成できる。ビア穴２８はレーザ光照射、エッチング等によって形成できる。

【００２８】図６(c)は前述した実施形態と同様な方法により、ビア穴２８にビア３２を形成し、ビア３２を介して下層の配線パターンと電気的に接続する上層の配線パターン２２を絶縁層２６の表面に形成した状態である。図６(d)は次に、絶縁層２６の上に第２層目の半導体素子１２を電極端子形成面を上面にして搭載した状態である。この第２層目の半導体素子１２は絶縁層２６の表面に形成した配線パターン２２の上に搭載することももちろん可能である。

【００２９】図６(d)は第２層目の半導体素子１２の側面間を絶縁層２６によって封止するとともに、配線パターン２２を絶縁層２６によって被覆した状態である。当該層における半導体素子１２の平面配置に合わせて素子収納孔を設けた絶縁性フィルムを用いることにより、前述したと同様な方法によって絶縁層２６を形成し、ビア穴２８を形成する。絶縁層２６の表面と半導体素子１２の電極端子形成面とは同一高さ面となっている。図６(e)は絶縁層２６と半導体素子１２の電極端子形成面に配線パターン２２を形成した状態である。配線パターン２２には半導体素子１２の電極端子と電気的に接続される接続パターン３４が設けられる。

【００３０】半導体素子１２をさらに上層に積層する場合は、上述したように、絶縁層２６を中間層に形成して積層していけばよい。図５はこうして作成した半導体装置を示すものである。前述したように、隣接する半導体素子１２の中間層に絶縁層２６を設けることにより、平面配置で見た場合、半導体素子１２を重複させて配置することができ、半導体装置の平面方向での集積度を効果的に向上させることが可能になる。

【００３１】本実施形態の半導体装置では基板３０に金属板を使用し、基板強度を高めて配線層、絶縁層を多層に形成した際の配線基板の反り等の変形を好適に防止できるようにしている。また、基板３０に金属板を使用することにより、基板３０からの熱放散性を向上させ、配線基板に埋設された半導体素子１２から発生する熱を効果的に放散することを可能にする。基板３０に金属板を使用することは半導体素子１２を多数個搭載するような場合に有効である。また、本実施形態のように基板３０の一方の面のみに配線層を設けた場合は、基板３０の他方の露出面に放熱フィンを取り付けて熱放散性をさらに改善することが可能になる。

【００３２】なお、上記各実施形態では、外部接続端子としてはんだボール５０を使用した例を示したが、はんだボールに限らずリードピン等を使用することも可能であり、実装構造は種々の形式を採用することができる。たとえば、外部接続用の端子部を保護めっきを施したコンタクト部に形成して実装基板側の接続電極に電気的に接続するように構成する方法、外部接続用の端子をエッジコネクタに形成する方法等がある。

【００３３】

【発明の効果】本発明に係る半導体装置は、上述したように、配線層を多層に形成するとともに多層に形成した内層に半導体素子を埋設したことによって、半導体素子をきわめて集積したかたちで半導体装置に搭載することを可能にする。各層に形成される配線パターンに設けた接続パターンを介して半導体素子と配線パターンとが電気的に接続されるから、半導体素子と配線パターンとの電気的接続もきわめてコンパクトになされる。また、本発明に係る半導体装置の製造方法によれば、層間で配線パターンを確実に電気的に接続するとともに、半導体素子との電気的接続を確実にとって内層に半導体素子を埋設した多層の配線基板を確実に形成でき信頼性の高い、コンパクトな半導体装置を製造することができる。

【図面の簡単な説明】

【図１】本発明に係る半導体装置の製造方法を示す説明図である。

【図２】本発明に係る半導体装置の製造方法を示す説明図である。

【図３】基板に絶縁樹脂フィルムを圧着する方法を示す説明図である。

【図４】本発明に係る半導体装置の構成を示す断面図である。

【図５】本発明に係る半導体装置の他の実施形態の構成

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を示す断面図である。

【図６】半導体装置の他の実施形態の製造方法を示す説明図である。

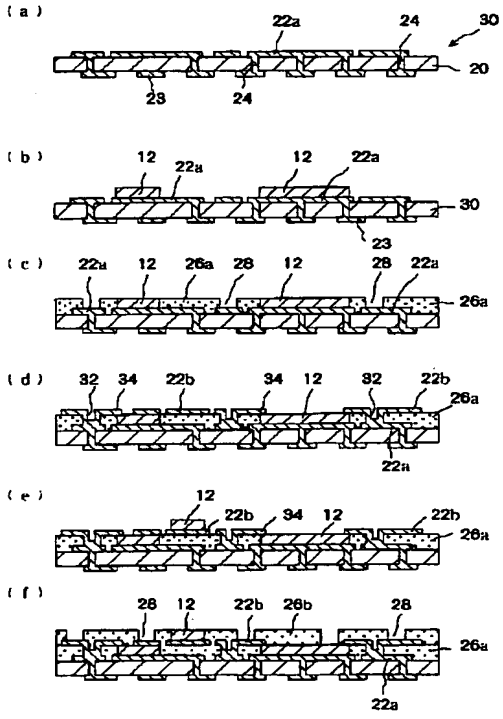
【図７】半導体素子を複数個搭載した半導体装置の従来例を示す断面図である。

【図８】半導体素子を複数個搭載した半導体装置の従来例を示す断面図である。

【符号の説明】

１０　基板
１２　半導体素子
１４　樹脂基体
１６　配線層
２０　樹脂基板
２２、２２ａ、２２ｂ、２２ｃ、２２ｄ　配線パターン＊
＊２３　配線パターン
２３ａ　ランド
２６、２６ａ、２６ｂ、２６ｃ　絶縁層
２８　ビア穴
３０　基板
３２　ビア
３４　接続パターン
３６　ソルダーレジスト
３８　接続部
４０ａ　素子収納孔
４０　絶縁樹脂フィルム
４２　リリースフィルム
４４　熱板
５０　外部接続端子

【図１】



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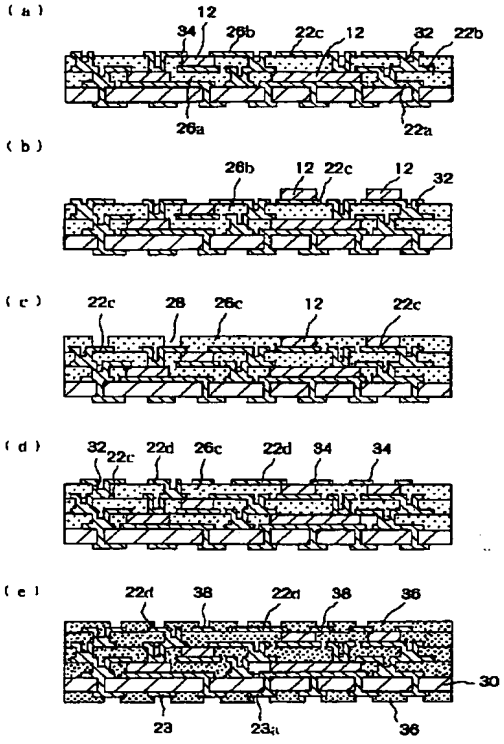

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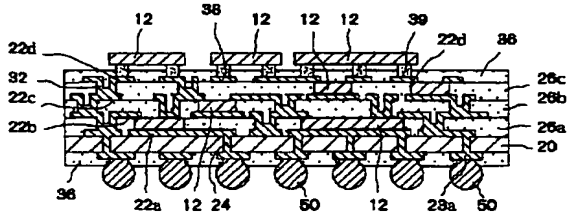

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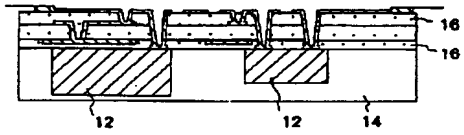

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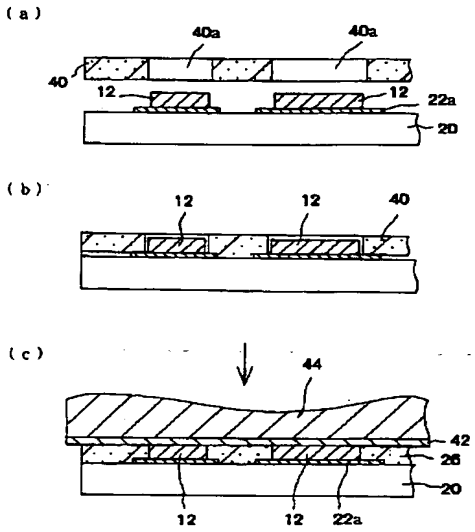
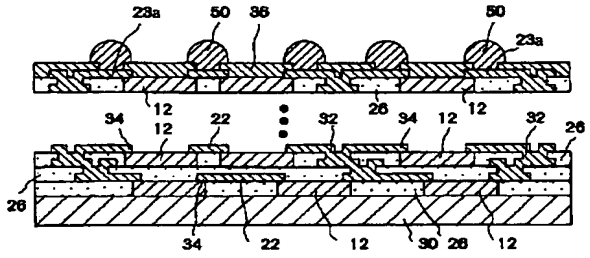
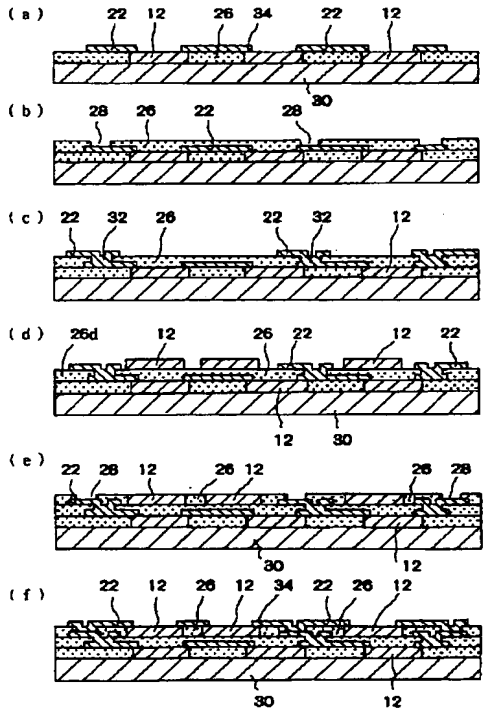

(a)
40a
40a
40
12
12
22a
20
(b)
12
12
40
(c)
44
42
26
20
12
12
22a

【図５】


23a
50
36
50
23a
12
26
12
34
12
22
32
32
34
12
26
26
34
22
12
30
26
12

【図６】


(a)
22
12
26
34
22
12
30
(b)
28
26
22
28
(c)
22
32
26
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32
12
(d)
26d
12
26
22
12
22
12
30
(e)
22
28
12
26
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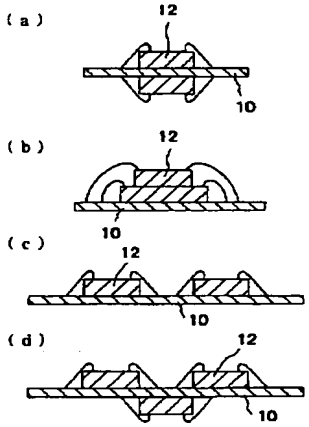
12
(f)
22
12
26
12
34
22
26
12
30
12

【図７】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12
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(b)
12
10
(c)
12
10
(d)
12
10

フロントページの続き

(51)Int.Cl.'	識別記号	Ｆ Ｉ	ﾃｰﾏｺｰﾄﾞ (参考)
Ｈ０５Ｋ 3/46			

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H01L 23/12
H01L 25/065
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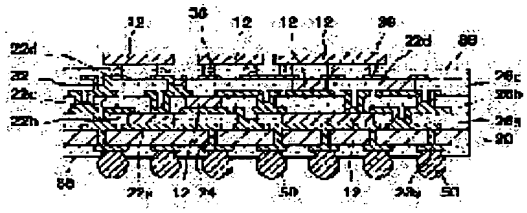
(71)Applicant : SHINKO ELECTRIC IND CO LTD
(72)Inventor : TAKEUCHI YUKIHARU

(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To load a semiconductor device by integrating semiconductor elements, and to provide a compact semiconductor device having a composite function.
SOLUTION: Wiring patterns 22a, 22b, 22c, and 22d are limited in multiple layers through insulating layers 26a, 26b, and 22c on a substrate 30, and the wiring patterns are electrically connected in the layers in this semiconductor device. In this case, semiconductor elements 12 electrically connected with the wiring patterns are embedded and loaded in wiring layers in the inner layers in which the wiring patterns are formed. The wiring layers in the inner layers are provided with the insulating layers 26a, 26b, 26c, and 26d with almost the same thickness as the thickness of the semiconductor elements for covering the wiring patterns in the lower layer, and for sealing the side faces of the semiconductor elements loaded in the inner layers with the electrode terminal formation faces as the upper faces, and the wiring patterns in the upper layer electrically connected through a via 32 formed through the insulating layers with the wiring patterns in the lower layer, formed on the surface of the insulating layers, extended on the electrode terminal formation faces of the semiconductor elements, and electrically connected with the electrode terminals.



LEGAL STATUS
[Date of request for examination]
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[Date of final disposal for application]
[Patent number]
[Date of registration]
[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device which the laminating of the circuit pattern is carried out to a multilayer through an insulating layer, and is characterized by laying the semiconductor device electrically connected with this circuit pattern under the wiring layer of the inner layer in which said circuit pattern was formed, and being carried in it in the semiconductor device which it comes to connect at a substrate top electrically [this circuit pattern] between layers.
[Claim 2] the thickness of a semiconductor device in which the wiring layer of a inner layer closes the side face of the semiconductor device which used the electrode terminal forming face as the top face, and was carried in the inner layer while covering a lower layer circuit pattern, and abbreviation -- with the insulating layer of the same thickness While connecting with a lower layer circuit pattern electrically through the beer formed by penetrating this insulating layer The semiconductor device according to claim 1 characterized by having the upper circuit pattern which is formed in the front face of this insulating layer, extends on the electrode terminal forming face of said semiconductor device, and is electrically connected with this electrode terminal.
[Claim 3] The semiconductor device according to claim 1 or 2 characterized by connecting electrically the circuit pattern prepared in both sides of a substrate through the flow section which said circuit pattern was formed in both sides of a substrate, and penetrated and formed the substrate.
[Claim 4] The semiconductor device according to claim 1 or 2 characterized by forming a substrate by the metal plate and forming the wiring layer which laid the semiconductor device under the inner layer by the side of one field of this metal plate.
[Claim 5] In the manufacture approach of a semiconductor device that the semiconductor device electrically connected with this circuit pattern was laid underground and carried in the wiring layer of the inner layer in which the circuit pattern was formed Use an electrode terminal forming face as a top face, and a semiconductor device is carried in the wiring layer which has a lower layer circuit pattern. The beer hole in which a lower layer circuit pattern and the side face of a semiconductor device are covered with an insulating layer, this insulating layer is penetrated, and said lower layer circuit pattern is exposed is formed. After forming the plating electric supply layer for electrolysis plating in the inside of a beer hole, the front face of an insulating layer, and the front face of a semiconductor device, The resist pattern which exposed the part which forms a circuit pattern on this plating electric supply layer is formed, and electrolysis plating is performed by using this resist pattern as a mask. Subsequently After removing said resist pattern, a part for the plating electric supply layer exposed by removal of this resist pattern is removed. The manufacture approach of the semiconductor device characterized by forming the beer which connects electrically a lower layer circuit pattern and the upper circuit pattern, and the upper circuit pattern electrically connected with the electrode terminal of said semiconductor device.
[Claim 6] In the manufacture approach of a semiconductor device that the semiconductor device electrically connected with this circuit pattern was laid underground and carried in the wiring layer of the inner layer in which the circuit pattern was formed Make an electrode terminal forming face the insulating layer which covered and formed the substrate or the lower layer circuit pattern on the top face, and a semiconductor device is carried. The beer hole in which the side face of a semiconductor device is covered with an insulating layer, this insulating layer is penetrated, and said lower layer circuit pattern is exposed is formed. After forming the plating electric supply layer for electrolysis plating in the inside of a beer hole, the front face of an insulating layer, and the front face of a semiconductor device, The resist pattern which exposed the part which forms a circuit pattern on this plating electric supply layer is formed, and electrolysis plating is performed by using this resist pattern as a mask. Subsequently After removing said resist pattern, a part for the plating electric supply layer exposed by removal of this resist pattern is removed. The manufacture approach of the semiconductor device characterized by forming the beer which connects electrically a lower layer circuit pattern and the upper circuit

pattern, and the upper circuit pattern electrically connected with the electrode terminal of said semiconductor device.

[Claim 7] the thickness of the semiconductor device after carrying a semiconductor device in a predetermined location, and abbreviation — the manufacture approach of the semiconductor device according to claim 5 characterized by to form an insulating layer in the layer in which the alignment of a semiconductor device and the component receipt hole carried out, the insulating resin film with which it was formed in the same thickness and the component receipt hole which contains a semiconductor device was formed has arranged, a release film minded, said insulating resin film heated and pressurized, and a semiconductor device carried.

[Translation done.]

* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor device which carried two or more semiconductor devices in the single package, and its manufacture approach.
[0002]
[Description of the Prior Art] The semiconductor device which carried two or more semiconductor devices in the single package in order to attain high integration of a semiconductor device and advanced features is offered conventionally. Drawing 7 shows the example of the semiconductor device which carried two or more semiconductor devices 12 in one substrate 10. Drawing 7 (a) The example and drawing 7 (b) which carried the semiconductor device 12 in both sides of a substrate 10 The example and drawing 7 (c) which accumulated and carried the semiconductor device 12 in one side of a substrate 10 The example and drawing 7 (d) which carried two or more semiconductor devices 12 in the flat surface of a substrate 10 While carrying a semiconductor device 12 in both sides of a substrate 10, it is the example which carried two or more semiconductor devices 12 in the flat surface of a substrate.
[0003] The circuit pattern is formed in the front face of a substrate 10, and each has connected the semiconductor device 12 and the circuit pattern electrically by wirebonding in the example of illustration. Of course, the electrical installation of a semiconductor device 12 and a circuit pattern can use not only wirebonding connection but flip chip bonding, TAB connection, etc.
[0004]
[Problem(s) to be Solved by the Invention] Since the above-mentioned semiconductor device carries a semiconductor device 12 in the loading side of a substrate 10, the number of loading of a semiconductor device 12 is restricted, and even when it accumulates and carries a semiconductor device 12, the laminating of it cannot be carried out how many sheets. Moreover, when connecting a semiconductor device 12 and the circuit pattern of a substrate 10 by wirebonding, since bonding area is needed, the area which carries a semiconductor device 12 further becomes narrow.
[0005] Thus, when it carries two or more semiconductor devices 12 in a package, by the approach of only carrying a semiconductor device 12 in the loading side of a substrate 10, the number of loading of a semiconductor device 12 is limited, and sufficient high integration and advanced features cannot be attained. Then, the semiconductor device of the format which multilayers a substrate and builds in a semiconductor device in a substrate as an approach of attaining high integration and advanced features of a semiconductor device further is considered. Drawing 8 is a semiconductor device which lays a semiconductor device 12 underground into a resin matrix 14, forms a wiring layer 16 and changes on the electrode terminal forming face of a semiconductor device 12.
[0006] Thus, if the structure of the multilayer substrate equipped with two or more wiring layers is used, it is possible to connect mutually electrically and to arrange the components of the shape of a chip, such as a semiconductor device, in three dimension within a substrate. However, it is not necessarily easy to lay a semiconductor device underground in a substrate and to form a wiring layer in a multilayer, and it makes the whole thickness thin and also has the problem that a semiconductor device must be formed in a compact. The place which this invention requires for the semiconductor device which carried two or more semiconductor devices in such a single package, and is made into the purpose can attain high integration and advanced features effectively compared with the conventional semiconductor device, and is to offer certainly the semiconductor device which can be manufactured in a compact, and its manufacture approach.
[0007]

[Means for Solving the Problem] This invention is equipped with the next configuration in order to attain the above-mentioned purpose. That is, the laminating of the circuit pattern is carried out to a multilayer through an insulating layer, and it is characterized by laying the semiconductor device electrically connected with this circuit pattern under the wiring layer of the inner layer in which said circuit pattern was formed, and being carried in it in the semiconductor device which it comes to connect at a substrate top electrically [this circuit pattern] between layers. moreover, the thickness of a semiconductor device in which the wiring layer of a inner layer closes the side face of the semiconductor device which used the electrode terminal forming face as the top face, and was carried in the inner layer while covering a lower layer circuit pattern and abbreviation -- with the insulating layer of the same thickness While connecting with a lower layer circuit pattern electrically through the beer formed by penetrating this insulating layer, it is characterized by having the upper circuit pattern which is formed in the front face of this insulating layer, extends on the electrode terminal forming face of said semiconductor device, and is electrically connected with this electrode terminal. Moreover, said circuit pattern is formed in both sides of a substrate, and it is characterized by connecting electrically the circuit pattern prepared in both sides of a substrate through the flow section which penetrated and formed the substrate. Moreover, it is characterized by forming a substrate by the metal plate and forming the wiring layer which laid the semiconductor device under the inner layer by the side of one field of this metal plate.

[0008] Moreover, it sets to the manufacture approach of a semiconductor device that the semiconductor device electrically connected with this circuit pattern was laid underground and carried in the wiring layer of the inner layer in which the circuit pattern was formed. Use an electrode terminal forming face as a top face, and a semiconductor device is carried in the wiring layer which has a lower layer circuit pattern. The beer hole in which a lower layer circuit pattern and the side face of a semiconductor device are covered with an insulating layer, this insulating layer is penetrated, and said lower layer circuit pattern is exposed is formed. After forming the plating electric supply layer for electrolysis plating in the inside of a beer hole, the front face of an insulating layer, and the front face of a semiconductor device, The resist pattern which exposed the part which forms a circuit pattern on this plating electric supply layer is formed, and electrolysis plating is performed by using this resist pattern as a mask. Subsequently After removing said resist pattern, a part for the plating electric supply layer exposed by removal of this resist pattern is removed. It is characterized by forming the beer which connects electrically a lower layer circuit pattern and the upper circuit pattern, and the upper circuit pattern electrically connected with the electrode terminal of said semiconductor device. Moreover, make an electrode terminal forming face the insulating layer which covered and formed the substrate or the lower layer circuit pattern in the manufacture approach of said semiconductor device on the top face, and a semiconductor device is carried. The beer hole in which the side face of a semiconductor device is covered with an insulating layer, this insulating layer is penetrated, and said lower layer circuit pattern is exposed is formed. After forming the plating electric supply layer for electrolysis plating in the inside of a beer hole, the front face of an insulating layer, and the front face of a semiconductor device, The resist pattern which exposed the part which forms a circuit pattern on this plating electric supply layer is formed, and electrolysis plating is performed by using this resist pattern as a mask. Subsequently After removing said resist pattern, a part for the plating electric supply layer exposed by removal of this resist pattern is removed. It is characterized by forming the beer which connects electrically a lower layer circuit pattern and the upper circuit pattern, and the upper circuit pattern electrically connected with the electrode terminal of said semiconductor device. moreover, the thickness of the semiconductor device after carrying a semiconductor device in a predetermined location and abbreviation -- it is characterized by to form an insulating layer in the layer in which alignment of a semiconductor device and the component receipt hole was carried out, the insulating resin film with which it was formed in the same thickness and the component receipt hole which contains a semiconductor device was formed has been arranged, the release film minded, said insulating resin film heated and pressurized, and a semiconductor device carried.

[0009]

[Embodiment of the Invention] Hereafter, the suitable operation gestalt of this invention is explained to a detail based on an accompanying drawing. Drawing 1 and 2 are the explanatory views showing the manufacture approach of the semiconductor device concerning this invention in order of a process. With this operation gestalt, a wiring layer is formed in a substrate at a multilayer using double-sided copper-clad ****** which stuck copper foil on both sides of a resin substrate. Although it is also possible to use a metal substrate, a metal core base material, etc. as a substrate in addition to a resin substrate, below, how to form a semiconductor device first using the substrate which uses a resin substrate as a substrate ingredient is explained.

[0010] Drawing 1 (a) Circuit patterns 22a and 23 are formed in one field of the resin substrate 20, and the field of another side, and the substrate 30 to which these circuit patterns 22a and 23 were electrically connected

through the flow section 24 which penetrates the resin substrate 20 in the thickness direction is shown. a substrate 30 -- double-sided copper-clad ****** -- a through tube -- forming -- non-electrolytic copper plating and electrolytic copper plating -- giving -- the internal surface of a through tube -- a conductor -- after forming the film and filling up a through tube with resin, the conductor layer which consists of a plating layer formed on copper foil by the surface copper foil and the plating of the resin substrate 20 is etched, and circuit patterns 22a and 23 are formed and it is obtained. the conductor formed in the internal surface of a through tube -- the film serves as the flow section 24 which connects circuit patterns 22a and 23 electrically.

[0011] In addition, a substrate 30 may have what formed the circuit pattern in both sides of the resin substrate 20 at two or more layers, for example, the wiring layer of four layers. A substrate 30 acts as a core substrate in a multilayer-interconnection substrate. After forming a lower layer circuit pattern, the substrate which formed the wiring layer in two or more layers covers a circuit pattern with an insulating layer, forms a beer hole in an insulating layer by laser beam exposure etc., puts the front face of an insulating layer including the inside of a beer hole by the conductor layer, etches a conductor layer into a necessary pattern, and is obtained. in addition, the internal surface of the through tube after making into the process after covering a circuit pattern with an insulating layer as an option the process which opens a through tube in a resin substrate and forming through tubes including an insulating layer -- a conductor -- there is also the approach of forming and uniting the section and forming a conductor layer on the surface of an insulating layer, and etching a conductor layer and forming the upper circuit pattern.

[0012] Drawing 1 (b) Next, it is in the condition which carried the semiconductor device 12 in the substrate 30. A semiconductor device 12 is carried in the wiring layer of the 1st layer by making a functional side into a top-face side. Circuit pattern 22a is formed in the predetermined pattern in consideration of electrical installation with the upper circuit pattern in consideration of the helicopter loading site of a semiconductor device 12. For example, it was able to be said that circuit pattern 22a was formed as the formation approach of circuit pattern 22a so that the loading section of a semiconductor device 12 may serve as touch-down potential. As shown in drawing, a semiconductor device 12 is carried in two or more places by flat-surface within the limits of a substrate 30.

[0013] The semiconductor device of this operation gestalt is formed so that the laminating of the semiconductor device 12 may be carried out only to one field of a substrate 30, and the circuit pattern 23 prepared in the inferior surface of tongue of a substrate 30 with this operation gestalt is formed as a land which joins external connection terminals, such as a solder ball. Of course, it is possible to carry a semiconductor device 12 in both sides of a substrate 30 according to a product gestalt. Since the laminating of the semiconductor device 12 is carried out and it is arranged in a substrate, it uses what has thickness thin as much as possible. The thing with a thickness of 50 micrometers - about 100 micrometers is offered as current and a semiconductor device. If it is the semiconductor device 12 of thickness of this level, it is fully possible to use it in a substrate, carrying out a laminating and laying underground.

[0014] Drawing 1 (c) Next, it is in the condition which covered circuit pattern of 1st layer 22a with insulating-layer 26a. 28 is a beer hole for forming the beer which connects a wiring layer electrically between layers. the time of forming insulating-layer 26a with this operation gestalt -- the thickness of a semiconductor device 12, and abbreviation -- it is the description to form insulating-layer 26a in the same thickness, and to form so that the electrode terminal forming face (top face) of a semiconductor device 12 may not be covered with insulating-layer 26a. A semiconductor device 12 and a circuit pattern are because it is made to connect electrically through the conductor layer formed in the front face of insulating-layer 26a.

[0015] In order to make it not cover the electrode terminal forming face of a semiconductor device 12 with insulating-layer 26a, the film which formed component receipt hole 40a according to the helicopter loading site of a semiconductor device 12 as an insulating resin film 40 which forms insulating-layer 26a is used. How to paste up the insulating resin film 40 on a substrate at drawing 3 is shown. Alignment of the insulating resin film 40 in which component receipt hole 40a was formed is carried out to a substrate (drawing 3 (a)), and it arranges to a substrate (drawing 3 (b)). Since component receipt hole 40a is formed in the insulating resin film 40, the insulating resin film 40 is arranged without covering the electrode terminal forming face of a semiconductor device 12.

[0016] After arranging the insulating resin film 40 to a substrate, the insulating resin film 40 is heated and pressurized and insulating-layer 26a is formed (drawing 3 (c)). This heating / pressurization actuation is aimed at pasting up the insulating resin film 40 certainly and making the front face of insulating-layer 26a into the front face of a semiconductor device 12, and the flat side of the same height. The release film 42 covers the front face of the insulating resin film 40 and a semiconductor device 12 with an operation gestalt, the release film 42 is minded, it heats and pressurizes with a hot platen 44, and the side-face part of a semiconductor device 12 is

closed. In case the insulating resin film 40 is heated and pressurized and it pastes up, thermocompression bonding is carried out through the release film 42, because the electrode terminal forming face of a semiconductor device 12 is not polluted.

[0017] The release film 42 has necessary thermal resistance, and uses the insulating resin film 40 (insulating-layer 26a), a semiconductor device 12, and the thing that can exfoliate easily. As an insulating resin film 40, the polyimide resin which has an adhesive property, for example can be used. component receipt hole 40a formed in the insulating resin film 40 -- a semiconductor device 12 and this ** -- or it forms a little greatly. Moreover, the insulating resin film 40 is the same as the thickness of a semiconductor device 12, or uses a little thick thing. After forming insulating-layer 26a, a laser beam is irradiated to the necessary part of insulating-layer 26a, and the beer hole 28 which circuit pattern 22a exposes to a base is formed. In this way, insulating-layer 26a in which the beer hole 28 shown in drawing 1 (c) was formed is obtained.

[0018] Drawing 1 (d) It is in the condition in which circuit pattern of 2nd layer 22b was formed on the front face of insulating-layer 26a. Circuit pattern of 2nd layer 22b can be formed by the following approaches. First, the thin conductive layer as a plating electric supply layer which performs electrolysis plating is formed in the front face of insulating-layer 26a which performs non-electrolytic copper plating or sputtering to insulating-layer 26a, and includes the beer hole 28, and the front face of a semiconductor device 12. Next, a photosensitive resist is applied to the front face of this thin conductive layer, and the resist pattern which exposed the part which forms circuit pattern of 2nd layer 22b is formed. Next, this resist pattern is used as the mask for plating, electrolytic copper plating is performed by using a thin conductive layer as a plating electric supply layer, and a thick conductor layer is formed. After forming a conductor layer, the resist pattern used with previous electrolysis plating is removed, etching removes the exposed part of a thin plating electric supply layer, and it leaves a thick conductor layer. In this way, circuit pattern 22b is formed in insulating-layer 26a.

[0019] In the beer hole 28, a conductor layer is put and formed in the inside of a hole, and the beer 32 which connects electrically circuit pattern of 1st layer 22a and circuit pattern of 2nd layer 22b is formed. Moreover, in the electrode terminal forming face of a semiconductor device 12, the connection pattern 34 electrically connected with the electrode terminal of a semiconductor device 12 is formed. The connection pattern 34 is formed so that it may extend on the electrode terminal forming face of a semiconductor device 12 and may connect with an electrode terminal. As mentioned above, since the front face of insulating-layer 26a and the electrode terminal forming face of a semiconductor device 12 are formed in the flat side of the same height, after forming the thin conductive layer for plating electric supply layers, the connection pattern 34 is formed in a circuit pattern and coincidence by performing electrolysis plating using the resist pattern for plating. In addition, the connection pattern 34 turns into some circuit patterns in the wiring layer concerned, and is called circuit pattern in the semantics containing both the connection patterns 34 connected to the pattern and semiconductor device 12 for leading about in the wiring layer concerned.

[0020] Drawing 1 (e) It is in the condition which carried the semiconductor device 12 in circuit pattern of 2nd layer 22b. Like the approach which carried the semiconductor device 12 in circuit pattern of 1st layer 22a, an electrode terminal forming face is used as a top face, alignment is carried out to circuit pattern 22b, and a semiconductor device 12 is carried. Drawing 1 (f) Next, it is in the condition which covered circuit pattern of 2nd layer 22b with insulating-layer 26b. It forms so that thermocompression bonding of the insulating resin film which prepared the component receipt hole to compensate for arrangement of a semiconductor device 12 may be carried out to insulating-layer 26b having formed insulating-layer 26a and the electrode terminal forming face of a semiconductor device 12 and the front face of insulating-layer 26b may be it with the flat side of the same height similarly. 28 is the beer hole formed in insulating-layer 26b.

[0021] Drawing 2 (a) It is in the condition in which circuit pattern 22c of the 3rd layer was formed on the front face of insulating-layer 26b. 32 is beer which connects electrically circuit pattern 22b of the 2nd layer, and circuit pattern 22c of the 3rd eye. The connection pattern 34 electrically connected with the electrode terminal of a semiconductor device 12 is formed in circuit pattern 22c like the case of the 2nd layer. Drawing 2 (b) It is in the condition which carried the semiconductor device 12 in circuit pattern 22c of the 3rd layer. An electrode terminal forming face is used as a top face also in this case, and a semiconductor device 12 is carried. Drawing 2 (c) It is in the condition which covered circuit pattern 22c with insulating-layer 26c. Insulating-layer 26c is formed so that the electrode terminal forming face of a semiconductor device 12 and the front face of insulating-layer 26c may turn into a flat-tapped flat side.

[0022] Drawing 2 (d) It is in the condition which formed the conductor layer in the front face of insulating-layer 26c, etched the conductor layer and formed 22d of circuit patterns of the 4th layer. It connects with circuit pattern of 3rd layer 22c electrically through beer 32, and 22d of circuit patterns of the 4th layer is also

electrically connected with a semiconductor device 12 through the connection pattern 34. Drawing 2 (e) After forming 22d of circuit patterns of the 4th layer, the front face of 22d of circuit patterns of the 4th layer is covered with the solder resist 36 of a protective coat, and the circuit pattern 23 of the inferior surface of tongue of a substrate 30 is covered with a solder resist 36. The solder resist 36 which covers the front face of 22d of circuit patterns forms the connection 38 which 22d of circuit patterns exposes on a base according to the arrangement location of the connection terminal of a semiconductor device carried in the maximum upper layer. On the other hand, the solder resist 36 which covers a circuit pattern 23 is formed so that land 23a may be exposed on a base. Protection plating, such as gilding, is performed to the front face of a connection 38 and land 23a.

[0023] Drawing 2 (e) Two or more wiring layers which the shown multilayer-interconnection substrate used the resin substrate 20 as the substrate while the semiconductor device 12 had been arranged at the inner layer, and connected electrically between layers were formed. Drawing 4 is drawing 2 (e). It is the shown multilayer-interconnection substrate, and a semiconductor device 12 is carried in 22d of circuit patterns of the maximum upper layer through a bump 39, and the last configuration of a semiconductor device where the solder ball was joined and obtained as an external connection terminal 50 to land 23a of a circuit pattern 23 is shown. While a wiring layer is formed on one field of the resin substrate 20 at a multilayer and a semiconductor device 12 is embedded into these wiring layers, the external connection terminal 50 electrically connected with these semiconductor devices 12 is attached in the field of another side of the resin substrate 20.

[0024] It becomes possible to offer this semiconductor device as a compact semiconductor device with which the degree of integration of a semiconductor device 12 is extremely attained by altitude, and an exterior has a compound function since the semiconductor device 12 is built in and constituted inside the wiring substrate by which multilayer formation was carried out, although it is that to which the semiconductor device 12 was carried in one field of a wiring substrate, and the external connection terminal for mounting was joined by the field of another side. Moreover, the conventional approach that the manufacture approach also forms a wiring layer in a multilayer through an insulating layer is used, the electrical installation of the semiconductor device 12 and circuit pattern which were laid underground into the wiring layer can be secured, and it becomes possible to acquire the necessary dependability as a semiconductor device.

[0025] Drawing 5 shows other operation gestalten of the semiconductor device concerning this invention. The semiconductor device shown in drawing 5 is characterized by to have joined the solder ball which is the external connection terminal 50 to the external surface of the wiring layer formed in the multilayer, and forming an insulating layer 26 between the layers of the adjoining wiring layer while it lays a semiconductor device 12 under the inner layer and forms a wiring layer only on one field of a substrate 30. By having formed the insulating layer 26 between the layers of the adjoining wiring layer, constraint of the arrangement location of the semiconductor device 12 in an adjacent layer is eased, and it becomes possible to consider as the plane configuration which a semiconductor device 12 overlaps in an adjacent layer.

[0026] Drawing 6 shows the process which manufactures the semiconductor device shown in drawing 5 . Drawing 6 (a) It is in the condition which carried the semiconductor device 12 in the substrate 30 by having made the electrode terminal forming face into the top-face side, closed between the side faces of a semiconductor device 12 by the insulating layer 26, and formed the circuit pattern 22 in the front face of an insulating layer 26, and the front face of a semiconductor device 12. The connection pattern 34 linked to the electrode terminal of a semiconductor device 12 is formed in a circuit pattern 22. Thus, a semiconductor device 12 can also be directly carried in a substrate 30. An insulating layer 26 is formed so that it may become the front face of a semiconductor device 12, and the flat side of the same height, while it arranges the insulating resin film 40 which formed the component receipt hole according to the arrangement location of a semiconductor device 12 on a substrate 30 like the operation gestalt mentioned above and closes the side face of a semiconductor device 12 heating and by pressurizing through a release film.

[0027] A circuit pattern 22 can be formed by preparing a plating electric supply layer in the front face of an insulating layer 26 and a semiconductor device 12, preparing the resist pattern for forming a circuit pattern 22 in the front face of a plating electric supply layer, performing electrolysis plating by using this resist pattern as a mask, removing a resist pattern, and etching and removing the exposed part of a thin plating electric supply layer. Drawing 6 (b) The field in which the circuit pattern 22 was formed is covered with an insulating layer 26, and the lower layer circuit pattern 22 is in the condition in which the beer hole 28 exposed on a base was formed. An insulating layer 26 covers the insulating resin film 40, and can form it by coating thinly the resin which has electric insulation. The beer hole 28 can be formed by a laser beam exposure, etching, etc.

[0028] Drawing 6 (c) It is in the condition which formed beer 32 in the beer hole 28, and formed in the front face

of an insulating layer 26 the upper circuit pattern 22 electrically connected with a lower layer circuit pattern through beer 32 by the same approach as the operation gestalt mentioned above. Drawing 6 (d) Next, it is in the condition which used the electrode terminal forming face as the top face, and carried the semiconductor device 12 of the 2nd layer on the insulating layer 26. Of course, this semiconductor device 12 of the 2nd layer can also be carried on the circuit pattern 22 formed in the front face of an insulating layer 26.

[0029] Drawing 6 (d) While closing between the side faces of the semiconductor device 12 of the 2nd layer by the insulating layer 26, it is in the condition which covered the circuit pattern 22 with the insulating layer 26. By using the insulating film which prepared the component receipt hole according to the plane configuration of the semiconductor device 12 in the layer concerned, by the same approach, an insulating layer 26 is formed and the beer hole 28 is formed with having mentioned above. The front face of an insulating layer 26 and the electrode terminal forming face of a semiconductor device 12 are the same height side. Drawing 6 (e) It is in the condition which formed the circuit pattern 22 in the electrode terminal forming face of an insulating layer 26 and a semiconductor device 12. The connection pattern 34 electrically connected with the electrode terminal of a semiconductor device 12 is formed in a circuit pattern 22.

[0030] When carrying out the laminating of the semiconductor device 12 to the upper layer further, as mentioned above, an insulating layer 26 is formed in an interlayer and should just carry out the laminating. Drawing 5 shows the semiconductor device created in this way. As mentioned above, when it sees by plane configuration by preparing the interlayer of the adjoining semiconductor device 12 an insulating layer 26, a semiconductor device 12 is overlapped, it can arrange and it becomes possible to raise effectively the degree of integration in the direction of a flat surface of a semiconductor device.

[0031] A metal plate is used for a substrate 30 and it enables it to prevent suitably deformation of the curvature of the wiring substrate at the time of raising substrate reinforcement and forming a wiring layer and an insulating layer in a multilayer etc. in the semiconductor device of this operation gestalt. Moreover, by using a metal plate for a substrate 30, the heat leakage nature from a substrate 30 is raised, and it makes it possible to radiate effectively the heat generated from the semiconductor device 12 laid under the wiring substrate. It is effective to use a metal plate for a substrate 30, when it carries many semiconductor devices 12. Moreover, when a wiring layer is prepared only in one field of a substrate 30 like this operation gestalt, it becomes possible to attach a radiation fin in the exposure of another side of a substrate 30, and to improve heat leakage nature further.

[0032] In addition, although each above-mentioned operation gestalt showed the example which used the solder ball 50 as an external connection terminal, it is possible not only a solder ball but to use a lead pin etc., and mounting structure can adopt various formats. For example, there are an approach of constituting so that the terminal area for external connection may be formed in the contact section which performed protection plating and it may connect with the connection electrode by the side of a mounting substrate electrically, the approach of forming the terminal for external connection in an edge connector, etc.

[0033]

[Effect of the Invention] The semiconductor device concerning this invention makes it possible to carry a semiconductor device in a semiconductor device in the form accumulated extremely by having laid the semiconductor device under the inner layer formed in the multilayer while it forms a wiring layer in a multilayer, as mentioned above. Since a semiconductor device and a circuit pattern are electrically connected through the connection pattern prepared in the circuit pattern formed in each class, the electrical installation of a semiconductor device and a circuit pattern is also made very compactly. Moreover, according to the manufacture approach of the semiconductor device concerning this invention, while connecting a circuit pattern electrically certainly between layers, the multilayer wiring substrate which took electrical installation with a semiconductor device certainly, and laid the semiconductor device under the inner layer can be formed certainly, and a reliable compact semiconductor device can be manufactured.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the explanatory view showing the manufacture approach of the semiconductor device concerning this invention.
[Drawing 2] It is the explanatory view showing the manufacture approach of the semiconductor device concerning this invention.
[Drawing 3] It is the explanatory view showing how to stick an insulating resin film by pressure in a substrate.
[Drawing 4] It is the sectional view showing the configuration of the semiconductor device concerning this invention.
[Drawing 5] It is the sectional view showing the configuration of other operation gestalten of the semiconductor device concerning this invention.
[Drawing 6] It is the explanatory view showing the manufacture approach of other operation gestalten of a semiconductor device.
[Drawing 7] It is the sectional view showing the conventional example of the semiconductor device which carried two or more semiconductor devices.
[Drawing 8] It is the sectional view showing the conventional example of the semiconductor device which carried two or more semiconductor devices.
[Description of Notations]
10 Substrate
12 Semiconductor Device
14 Resin Matrix
16 Wiring Layer
20 Resin Substrate
22, 22a, 22b, 22c, 22d Circuit pattern
23 Circuit Pattern
23a Land
26, 26a, 26b, 26c Insulating layer
28 Beer Hole
30 Substrate
32 Beer
34 Connection Pattern
36 Solder Resist
38 Connection
40a Component receipt hole
40 Insulating Resin Film
42 Release Film
44 Hot Platen
50 External Connection Terminal

[Translation done.]